UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,052,951 B2
APPLICATION NO. : 10/776394
DATED : May 30, 2006
INVENTOR(S) : Joo et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page,
Section 54 should read -- METHODS FOR FABRICATING FERROELECTRIC MEMORY DEVICES WITH ENHANCED FERROELECTRIC PROPERTIES --

Column 1,
Lines 1-4 should read -- METHODS FOR FABRICATING FERROELECTRIC MEMORY DEVICES WITH ENHANCED FERROELECTRIC PROPERTIES --

Column 11,
Line 59 should read -- surface of the upper insulating pattern is higher than a --

Column 12,
Line 1 should read -- after patterning the lower electrode layer, the ferroelectric layer and the upper electrode layer, forming a third --

Line 32 should read -- sequentially stacked iridium and titanium aluminum nitride --

Column 13,
Line 5 should read -- forming a lower insulating layer including a conductive plug --

Line 9 should read -- pattering the upper insulating layer to form an opening --

Line 45 should read -- **19.** The method of claim **15,** wherein forming a lower --

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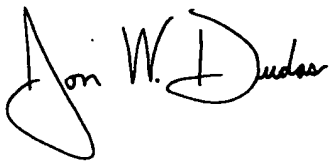
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 14,
Line 52 should read -- after patterning the lower electrode layer, the ferroelectric layer and the upper electrode layer, forming a third --

Signed and Sealed this

Fifth Day of December, 2006



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